IN THE ABSTRACT:

Please amend the abstract of the disclosure as follows:

A recovery clock synchronized with an internal clock faster than a system clock is obtained with an edge timing of the system clock output from a DUT. The present invention ~~is configured to comprise~~ includes: a time interpolator 20 which includes flip-flops ~~21a to 21n~~ (FF 21) which receive system clocks of the DUT 1, a delay circuit 22 which ~~sequentially receives strobes delayed at specified timing intervals to the FF 21 and~~ outputs time-series level data from the FF 21, and an encoder 28 which receives the time-series level data output ~~from the FF 21~~ and encodes it into positional data indicative of an edge timing; a digital filter 40 which includes a plurality of registers ~~41a to 41n~~ 41 which sequentially store the positional data ~~of the encoder 28~~ and output ~~it with a predetermined timing, and outputs~~ the positional data ~~from the register 41~~ as a recovery clock; and a data side selector 30 which selects output data of the DUT 1 ~~with~~ based on the recovery clock ~~being used as a selection signal~~.